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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,274	12/31/2003	Masanori Minamio	60188-692	6600

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,274	MINAMIO ET AL.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/19/04 & 12/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/748274 Attorney's Docket #: 60188-692
Filing Date: 12/31/03; claimed foreign priority to 12/5/01

Applicant: Minamio et al.

Examiner: Alexander Williams

Applicant's telephone interview with Nathan Flynn on 10/11/04 has been acknowledged. The election requirement of claims 1-9 has been withdrawn.

Applicant's Request for filing a Divisional Application filed 12/31/03 has been acknowledged in which claims 6-9 have been canceled.

This application is a divisional application of serial number 10/230297, filed 8/29/02.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 12/5/2001. It is noted, however, that applicant has not filed a certified copy of the foreign application as required by 35 U.S.C. 119(b).

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the semiconductor chip is mounted with its principal surface facing down; and the connection member is a bump made of a metal in claim 3 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 1 to 5 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is unclear and confusing to what is meant by and what shows "a die pad provided **by thinning a lower portion** of a lead frame; a semiconductor chip mounted on the die pad; a plurality of leads provided **by thinning an upper portion** of the lead frame." What defines thin or thinning? The die pad and leads appears to be the same size. How is they thinning?

In claim 3, it is unclear and confusing to how "semiconductor chip is mounted with its principal surface **facing down**; and the connection member **is a bump made of a metal**" with the previous claimed structure. Where is this shown in the drawings?

Any of claims 1 to 5 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2 and 5, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Shimaniki (U.S. Patent Application Publication # 2003/0001249 A1).

1. Shimanuki (figures 1 to 64) specifically figures 10(e) and 12 show a resin-encapsulated semiconductor device, comprising: a die pad **5** provided by thinning a lower portion of a lead frame; a semiconductor chip **8** mounted on the die pad; a plurality of leads **2** provided by thinning an upper portion of the lead frame; a connection member **10** for connecting the semiconductor chip and the lead with each other; a plurality of suspension leads **4** connected to the die pad; and an encapsulation resin **11** for encapsulating therein the die pad, the semiconductor chip, the leads, the connection member and the suspension leads, with a bottom surface and an outer side surface of each lead **(any portion of the leads outside of the resin 11)** being exposed as an external terminal, wherein: an upper surface **(top of 5)** of the die pad is located higher than an upper surface **(top of 2)** of the lead; and a lower surface **(bottom of 5)** of the die pad is located higher than a lower surface **(bottom of 2)** of the lead.

2. The resin-encapsulated semiconductor device of claim 1, Shimanuki show wherein: the semiconductor chip is mounted with its principal surface facing up **(top of 8)**; and the connection member is a thin metal wire.

5. The resin-encapsulated semiconductor device of claim 1, Shimanuki show wherein at least a portion of each of the die pad and the lead has a thickness of 100 micrometers to 150 micrometers **(page 12, paragraph [0192])**.

Claims 1 and 2, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Yamaguchi (Japan Patent # 11-260990).

1. Yamaguchi (figures 1 to 20) specifically figure 1 show a resin-encapsulated semiconductor device, comprising: a die pad **13** provided by thinning a lower portion **13b** of a lead frame; a semiconductor chip **15** mounted on the die pad; a plurality of leads **18** provided by thinning an upper portion **12** of the lead frame; a connection member **16** for connecting the semiconductor chip and the lead with each other; a plurality of suspension leads **14,45** connected to the die pad; and an encapsulation resin **17** for encapsulating therein the die pad, the semiconductor chip, the leads, the connection member and the suspension leads, with a bottom surface and an outer side surface of each lead being exposed as an external terminal, wherein: an upper surface of the die pad is located higher than an upper surface of the lead; and a lower surface of the die pad is located higher than a lower surface of the lead.

2. The resin-encapsulated semiconductor device of claim 1, Yamaguchi show wherein: the semiconductor chip is mounted with its principal surface facing up; and the connection member is a thin metal wire.

Claims 1, 3 and 4, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Wu (U.S. Patent # 6,661,087 B2).

1. Wu (figures 1 to 7) specifically figure 4 show a resin-encapsulated semiconductor device **3**, comprising: a die pad **31** provided by thinning a lower portion of a lead frame; a semiconductor chip **33** mounted on the die pad; a plurality of leads **32** provided by thinning an upper portion of the lead frame; a connection member **34** for connecting the semiconductor chip and

the lead with each other; a plurality of suspension leads **(inherit)** connected to the die pad; and an encapsulation resin **35** for encapsulating therein the die pad, the semiconductor chip, the leads, the connection member and the suspension leads, with a bottom surface and an outer side surface of each lead being exposed as an external terminal, wherein: an upper surface of the die pad is located higher than an upper surface of the lead; and a lower surface of the die pad is located higher than a lower surface of the lead.

3. The resin-encapsulated semiconductor device of claim 1, Wu show wherein: the semiconductor chip is mounted with its principal surface facing down; and the connection member is a bump **34** made of a metal.

4. The resin-encapsulated semiconductor device of claim 1, Wu show wherein at least a portion of the semiconductor chip overlaps with the lead **32,322** as viewed from above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/684,796,696,698,874,786,678,692,693,676,666,787	1/11/05
Other Documentation: foreign patents and literature in 257/684,796,696,698,874,786,678,692,693,676,666,787	1/11/05
Electronic data base(s): U.S. Patents EAST	1/11/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
1/11/05